

(use as many sheets as necessary)

Sheet	1	of	1
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Complete if Known

Application Number	10/040,940
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Filing Date	January 9, 2002
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First Named Inventor	Allon ADIR et al
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Group Art Unit	2857
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Examiner Name _____

Attorney Docket Number	ADIR=1
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U.S. PATENT DOCUMENTS

[illegible]

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²
XS	AC	A. CHANDRA, et al "AVGEN - A Test Generator for Architecture Verification" IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, Vol. 3, No. 2, pp. 188-200, June 1995.	
XS	AD	Yossi LICHTENSTEIN et al, "Model Based Test Generation for Processor Verification" IBM Israel Science and Technology, Sixth Innovative Applications of Artificial Intelligence Conference, August 1994, pp. 83-94.	

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Date
Considered

02/06/04

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